

Freeform Search

| | |
|--|--|
| Database: <input type="checkbox"/> US Pre-Grant Publication Full-Text Database <input type="checkbox"/> US Patents Full-Text Database <input checked="" type="checkbox"/> US OCR Full-Text Database <input type="checkbox"/> EPO Abstracts Database <input type="checkbox"/> JPO Abstracts Database <input type="checkbox"/> Derwent World Patents Index <input type="checkbox"/> IBM Technical Disclosure Bulletins | Term: (concurrent or simultaneous or parallel or contemporaneous) adj5 (access or accessing or reading or read or write or writing) adj5 12 adj5 |
| Display: <input type="text" value="10"/> Documents in <u>Display Format:</u> <input type="text"/> Starting with Number <input type="text" value="1"/> | |
| Generate: <input type="radio"/> Hit List <input checked="" type="radio"/> Hit Count <input type="radio"/> Side by Side <input type="radio"/> Image | |

Search History

DATE: Saturday, April 03, 2004 [Printable Copy](#) [Create Case](#)

| <u>Set</u> | <u>Name</u> | <u>Query</u> | <u>Hit</u> | <u>Set</u> |
|--------------|-------------|---|--------------|-------------|
| | | | <u>Count</u> | <u>Name</u> |
| side by side | | | | result set |
| | | DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ | | |
| <u>L33</u> | | (concurrent or simultaneous or parallel or contemporaneous) adj5 (access or accessing or reading or read or write or writing) adj5 l2 adj5 l3 | 21 | <u>L33</u> |
| <u>L32</u> | | L31 and l30 | 4 | <u>L32</u> |
| <u>L31</u> | | shared adj4 (address or control) adj4 bus | 569 | <u>L31</u> |
| <u>L30</u> | | (concurrent or simultaneous or parallel or contemporaneous) same (access or accessing or reading or read or write or writing) same l2 same l3 | 1018 | <u>L30</u> |
| <u>L29</u> | | L28 and (arbiter or arbitration or arbitrating) | 1 | <u>L29</u> |
| <u>L28</u> | | 5978866.pn. | 2 | <u>L28</u> |
| <u>L27</u> | | L26 same (arbitration or arbiter or arbitrator) same (MUX or multiplexor or multiplexer) | 31 | <u>L27</u> |
| <u>L26</u> | | shared adj4 bus | 5796 | <u>L26</u> |
| <u>L25</u> | | L22 same l21 same (MUX or multiplexor or multiplexer) | 1 | <u>L25</u> |
| <u>L24</u> | | L22 same l21 | 11 | <u>L24</u> |
| <u>L23</u> | | L22 and l21 | 21 | <u>L23</u> |
| <u>L22</u> | | (arbitration or arbiter or arbitrator) same address | 8124 | <u>L22</u> |

| | | | |
|------------|--|-------|------------|
| <u>L21</u> | shared adj4 address adj4 control adj4 bus | 40 | <u>L21</u> |
| <u>L20</u> | L19 and l11 | 8 | <u>L20</u> |
| <u>L19</u> | l12 same l13 same l1 | 207 | <u>L19</u> |
| <u>L18</u> | L17 and l11 | 59 | <u>L18</u> |
| <u>L17</u> | l12 same l13 same memory | 3486 | <u>L17</u> |
| <u>L16</u> | L15 and l11 | 1 | <u>L16</u> |
| <u>L15</u> | L14 same l13 same l12 | 3 | <u>L15</u> |
| <u>L14</u> | shared same (synchronous adj4 memory) | 229 | <u>L14</u> |
| <u>L13</u> | second adj2 (processor or cpu) | 18644 | <u>L13</u> |
| <u>L12</u> | first adj2 (processor or cpu) | 21893 | <u>L12</u> |
| <u>L11</u> | wireless adj3 system | 41160 | <u>L11</u> |
| <u>L10</u> | (DRAM or RAM or SDRAM) and l9 | 1 | <u>L10</u> |
| <u>L9</u> | 20040054845 | 1 | <u>L9</u> |
| <u>L8</u> | l1 same l2 same l6 | 191 | <u>L8</u> |
| <u>L7</u> | second adj2 bus | 14906 | <u>L7</u> |
| <u>L6</u> | first adj2 bus | 14710 | <u>L6</u> |
| <u>L5</u> | l1 same l2 same l3 same l4 | 3 | <u>L5</u> |
| <u>L4</u> | (dedicated or private or (non adj shared)) adj bus | 1642 | <u>L4</u> |
| <u>L3</u> | second adj2 memory | 56523 | <u>L3</u> |
| <u>L2</u> | first adj2 memory | 64834 | <u>L2</u> |
| <u>L1</u> | memory adj2 (control unit or controller) | 62229 | <u>L1</u> |

END OF SEARCH HISTORY